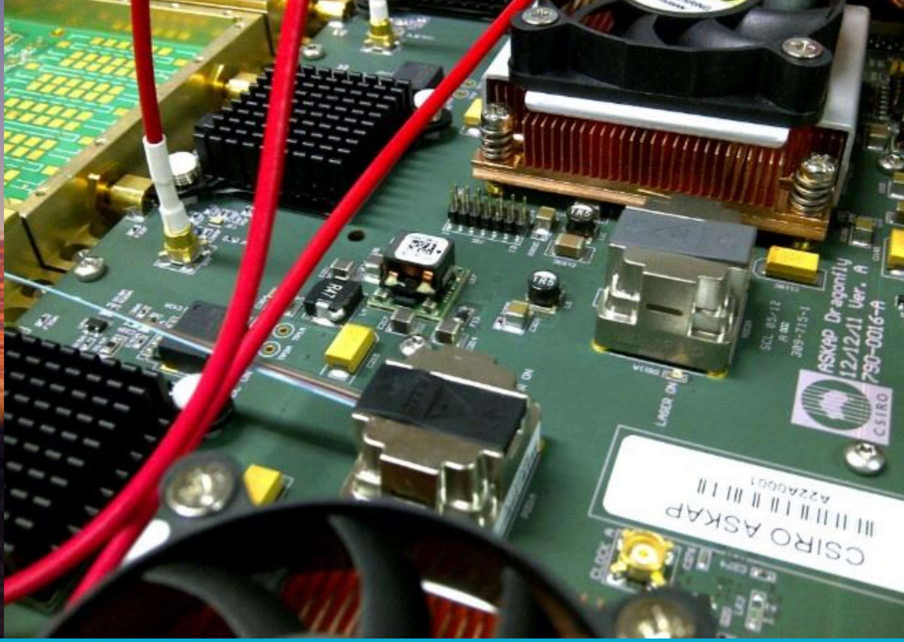


ASKAP Phased Array Feed Digital Beamformer

Design Overview and Performance Characteristics

John Tuthill, Tim Bateman, Grant Hampson, John Bunton, Andrew Brown, Daniel George, Mia Baquiran

August 2016

Outline:

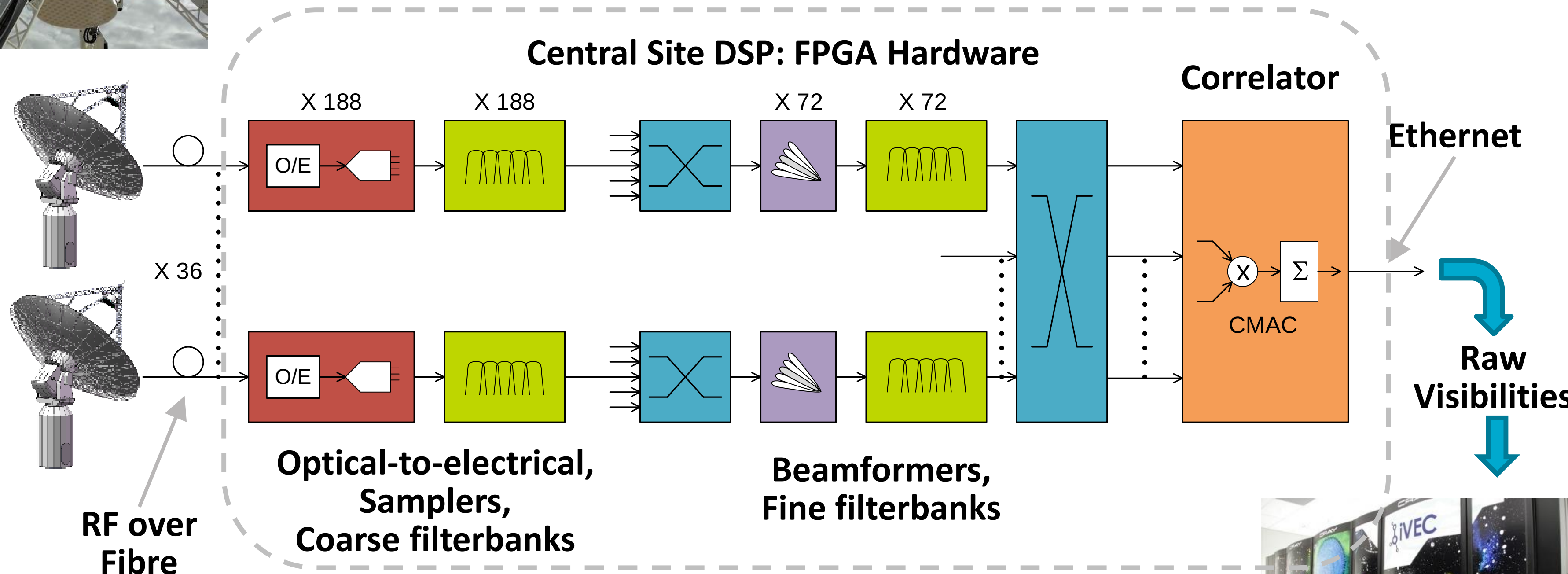
- ASKAP digital signal processing overview
- ASKAP digital beamformer
  - design
  - performance
- Current and future work

ASKAP: Architecture and signal chain

Mk-II PAF: checkerboard array, LNAs, RF filters, laser drivers

Custom digital system:

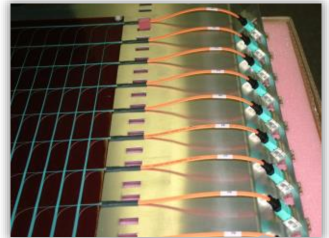
- Raw data ingest: 130Tbits/s
- Raw processing power: 2.3PMAC's/s

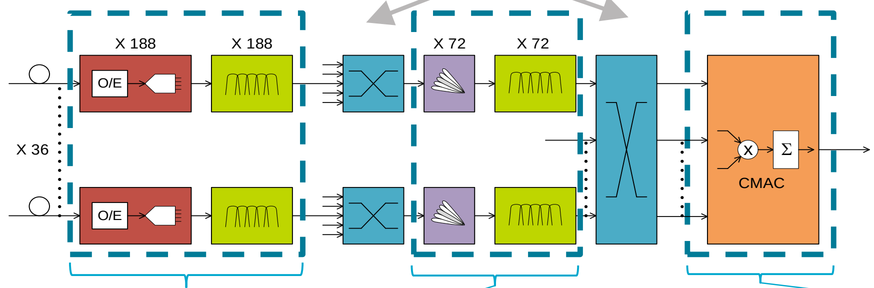


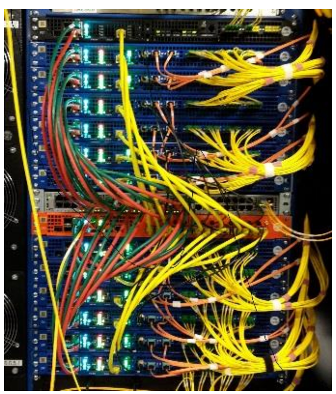
Imaging pipeline : iVEC "Galaxy"
Cray Inc. XC30 series supercomputer
Located in Perth, ~800km from MRO.
~200 TeraFLOPS

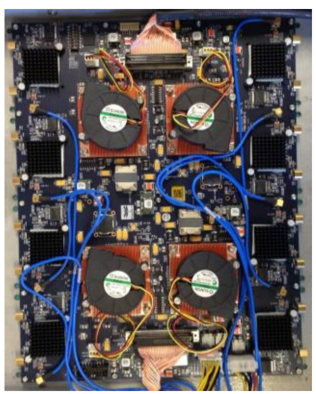
ASKAP DSP Hardware

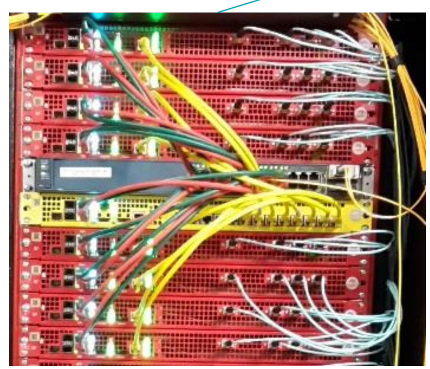
Passive optical circuits for data cross-connects

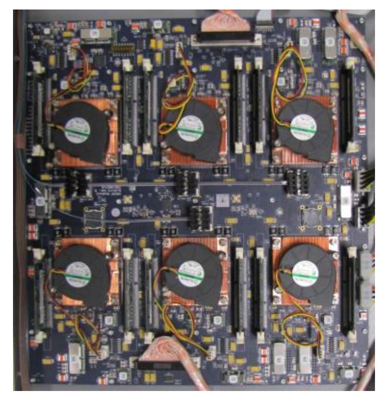






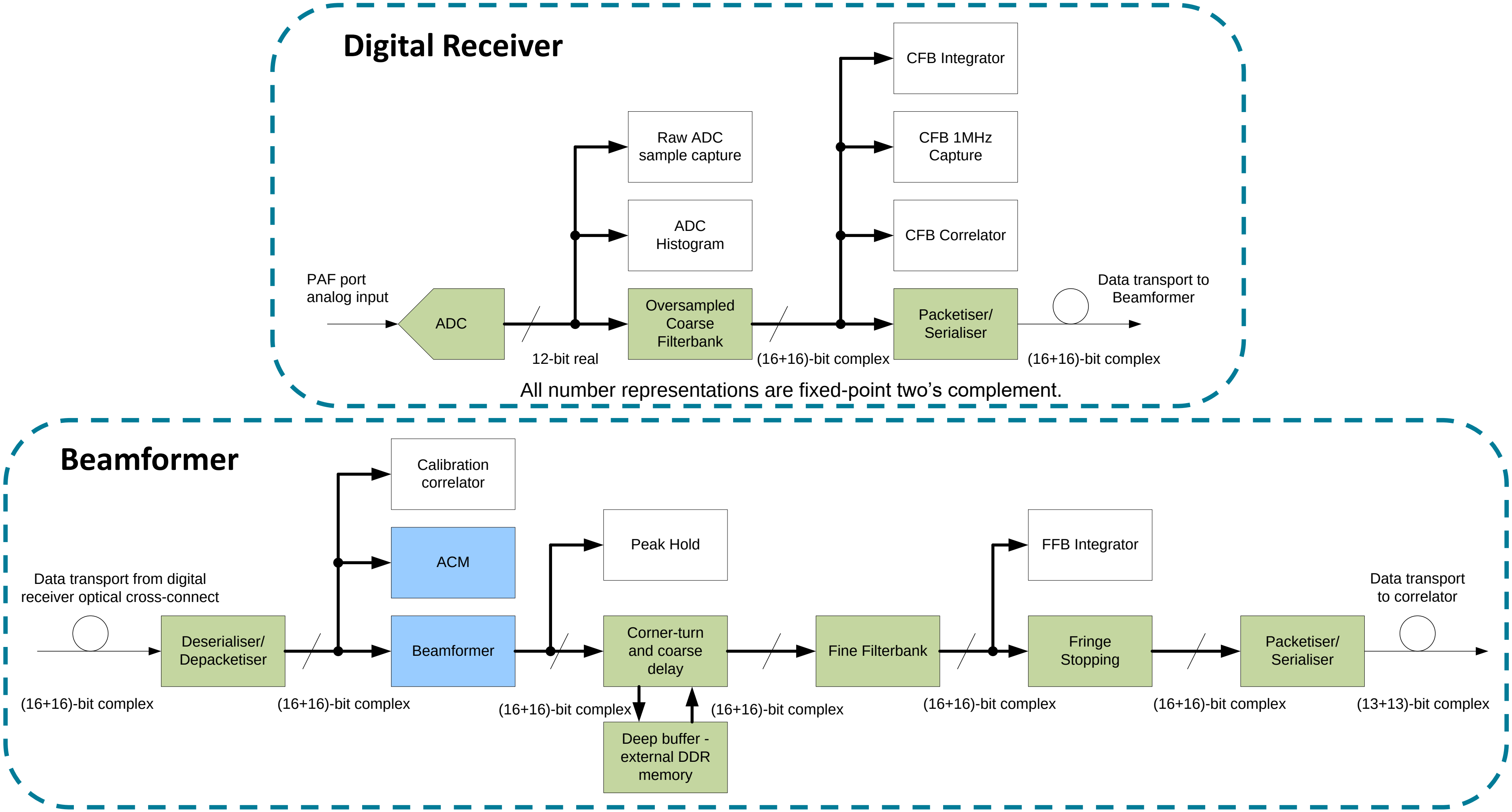






Dragonfly-3 Digital Receiver **Beamformer** ← **Redback-3 platform** → **Correlator**

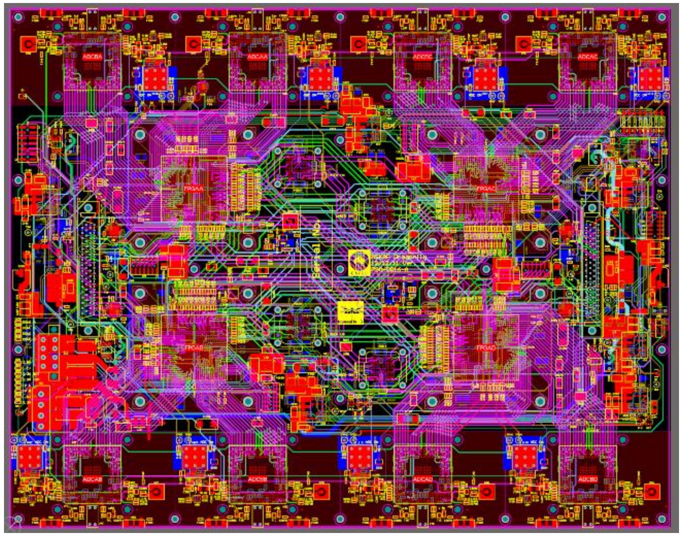
Detailed Signal Path – single PAF



Number representation is fixed-point signed two's complement throughout

ASKAP FPGA DSP Stat's – digital reveiver

- Sampling
  - ADC part - Nat. Semi. (now TI) ADC12D1600
  - Resolution 12bits (9.4 ENOB)
  - Analog BW 2.8GHz
  - Direct digital down-conversion (2^{nd} and 3^{rd} Nyquist zones)
  - Sample rates: 1,280MSps and 1,536MSps
  - 3 overlapping sampling bands between 700MHz and 1,800MHz
- Coarse frequency channelization
  - Processed bandwidth: 384 MHz
    (arbitrarily selectable anywhere in the observing band)
  - Coarse frequency channels: 1MHz **oversampled by 32/27**
  - Spectral flatness: <0.2dB
  - Sub-band alias rejection: >60dB

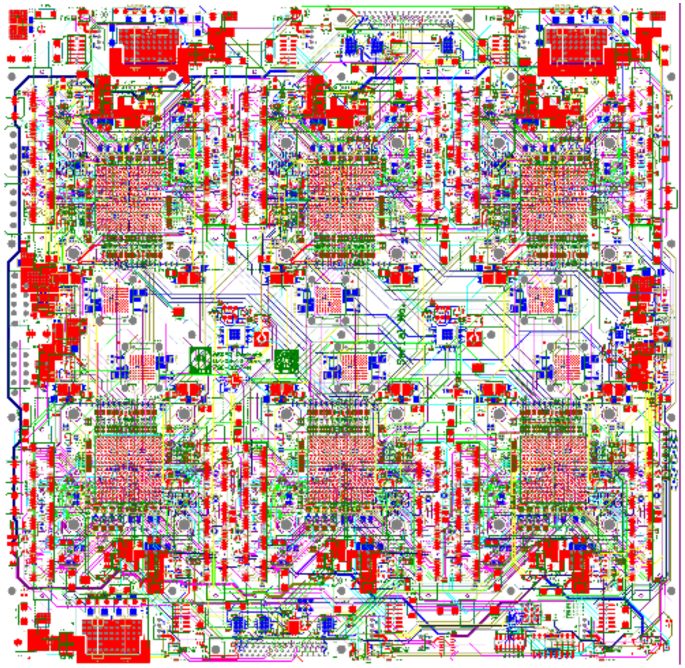


Dragonfly-3 Digital Receiver

ASKAP FPGA Hardware Stat’s – beamformer

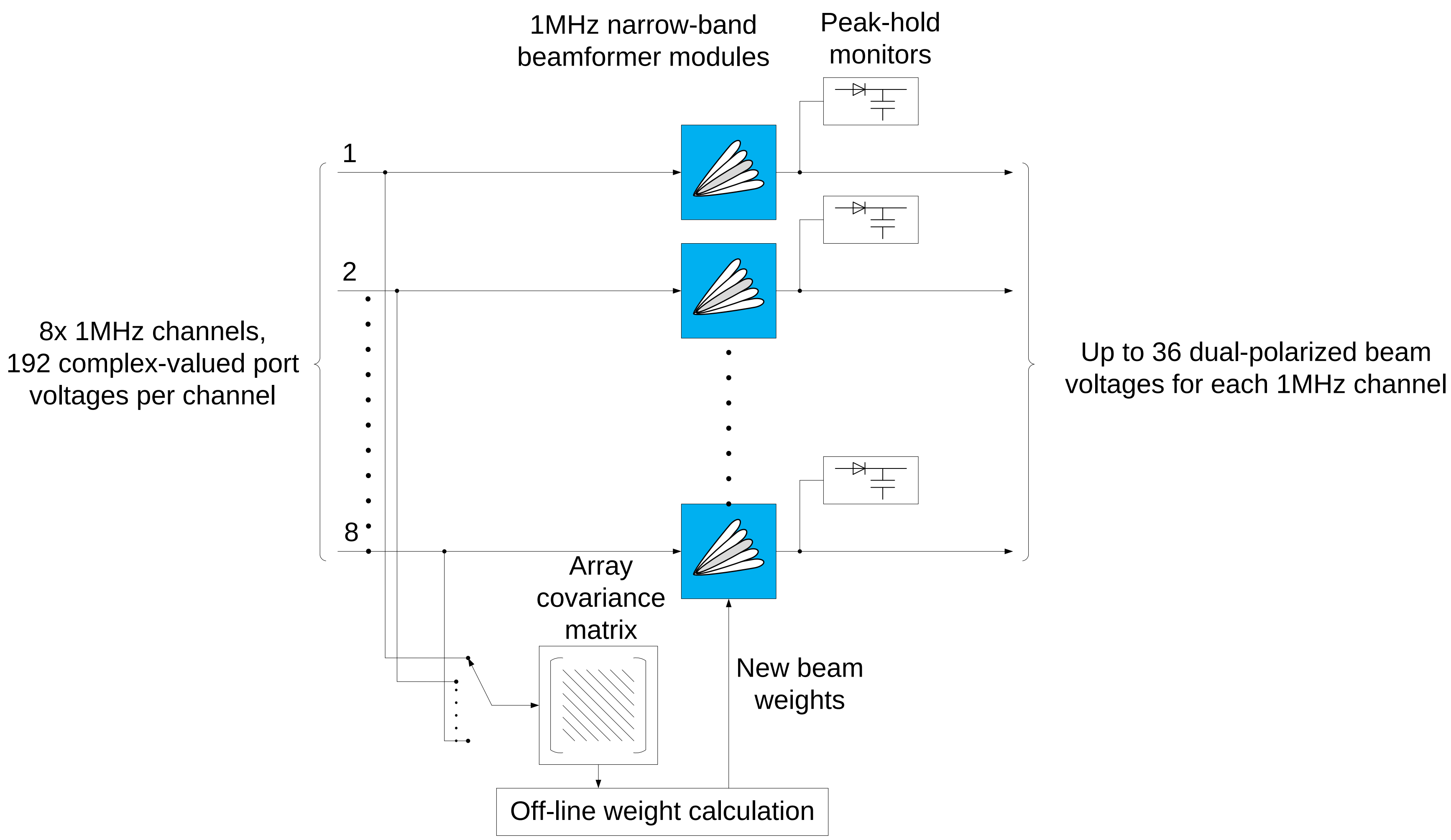
- Digital beamforming
  - Narrow-band beamformer structure (weight-and-sum)
  - Full 192x192 element array covariance matrix for all 1MHz coarse channels (floating-point O/P)
  - Up to 72 single-polarized beams (usually configured as 36 dual-pol beams)
- Fine frequency channelization
  - 6 frequency “zoom” modes:

    18.5kHz, 9.3kHz, 4.6kHz, 2.3kHz, 1.2kHz, 580Hz
  - Critically sampled (but not for long)
- Delay tracking and fringe-stopping
  - Coarse delay to 1us resolution
  - Time-varying phase slope applied to fine channels

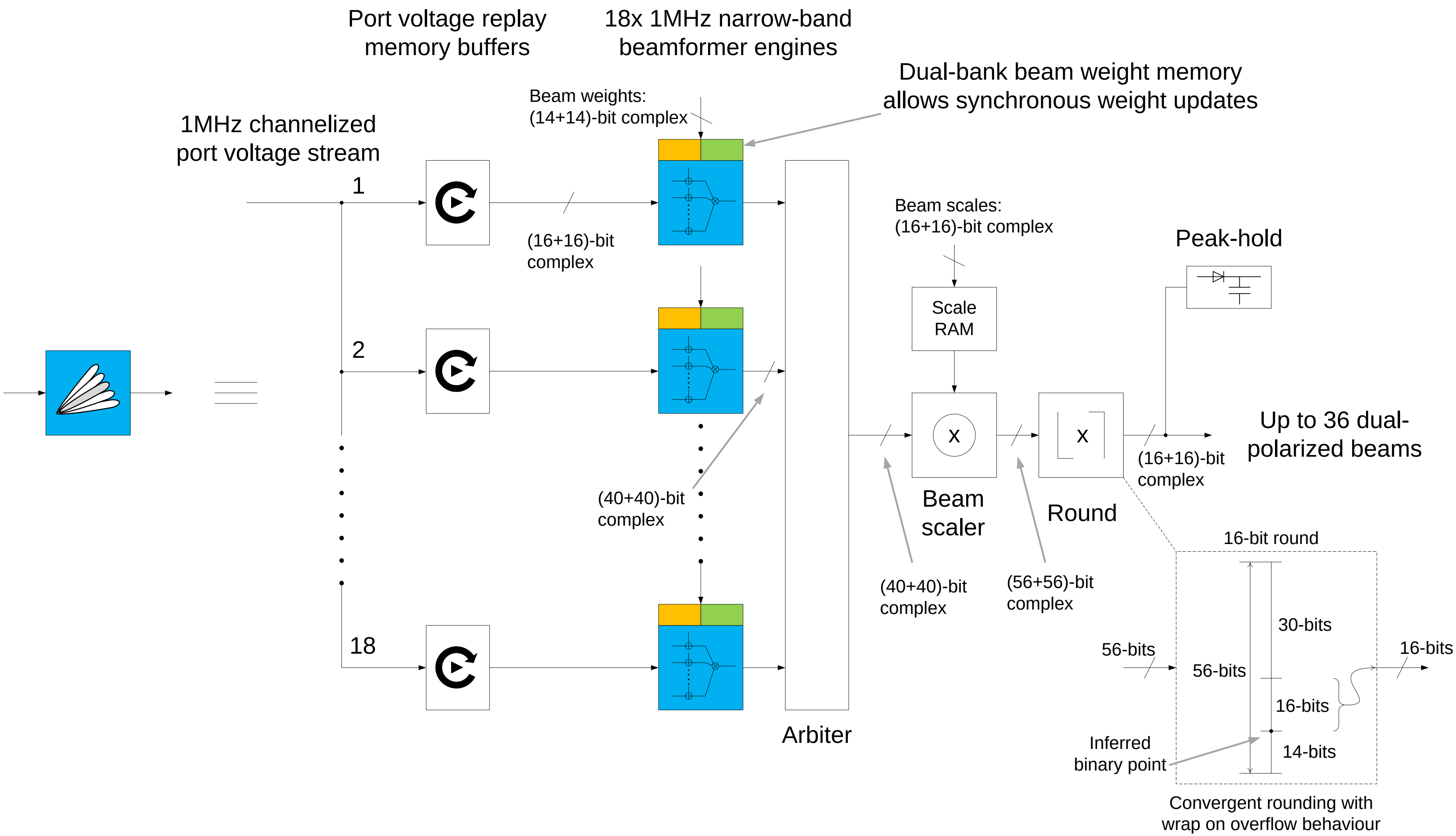


Redback-3 DSP Platform

Digital Beamformer (single DSP FPGA)



Individual 1MHz digital beamformer module



Beamformer engine performance

- Two main performance bounds:
  - Degrees of freedom in beam weight selection (architecture)
  - Maximum beam weight update rate (interface)

- 1. Degrees of freedom (# active weights)
  - Sample rate = 1MHz x 32/27 -> T = 843.75ns
  - Beamformer logic clock = 312.5MHz

→ All contributing PAF port voltages must be processed in 263 clocks

  - 18 physical instances of the beamformer process ~1 port voltage per clock cycle

→
- **18** single-pol beams: all **192** ports active
- **36** single-pol beams (1 replay): **130** active ports
- **72** single-pol beams (2 replays): **60** active ports

→ Implications for sidelobe control, null-steering, spill-over control

Beamformer engine performance

- 2. Maximum weight update rate, determined by:
  - ACM dump time
  - Beam weight upload time

  - ACM data volume and dump time:

    192 x 192 ports ÷ 2 (conjugate symmetry) x 2re/im x 32-bit float

    ≈172kBytes

    Measured ACM dump time ≈ 4ms/ACM (172kB/4ms = 43MB/s = 344Mb/s)

    (More efficient to stream raw port voltages than ACMs for dump times < 0.2ms)
  - **Beam weight upload time ≈ 180ms/chassis** (36 dual-pol beams, measured)

    Max "dynamic" beamforming period ≈ 48 x 4ms + 180ms ≈ **400ms**

    (does not include off-line weight calculation)

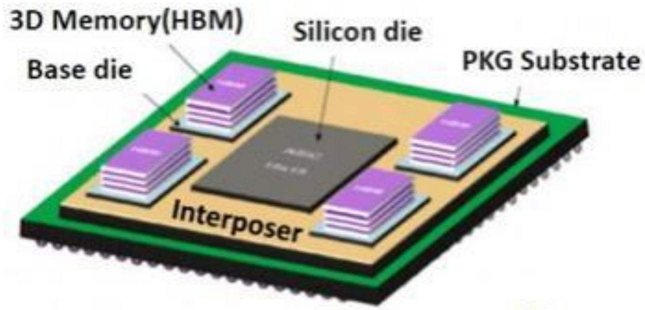
→ Implications for real-time/adaptive beamforming and RFI tracking

Current/future work (SKA.CSP)

Strong collaboration with ASTRON and AUT

- Physical aspects size/weight, power/cooling important
  - Liquid cooled heatsinks are better for RFI shielding
- Choice of on-board optics (short range MMF vs long range SMF)
- Integrated control and monitoring functions on the DSP FPGA
- Higher processing bandwidth and more beams
  - Not so much a limiting factor now as devices are much larger
- Larger devices
  - "Local" control loops
  - Capacity to calculate weights (dynamic beamforming)
- Need more memory (external and internal)
  - Large/fast corner-turns and transient buffers
- Higher reliability -> lower component count
- Scalable/flexible systems
  - Ability to trade of Beams, bandwidth and PAF ports

16nm process

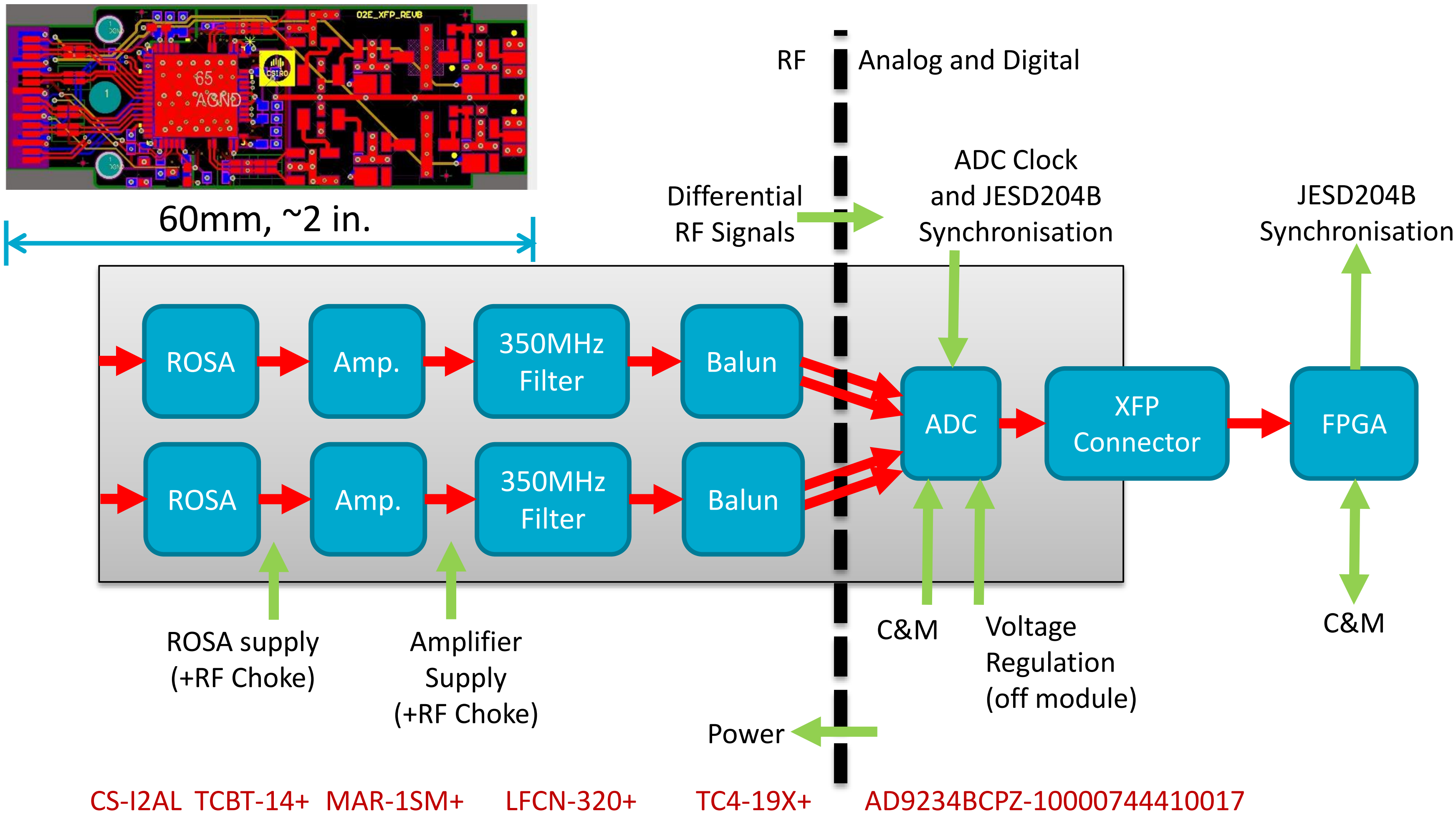


DSP algorithms and other work

- Algorithms and firmware
  - Fast ACM dumps/weight uploads
  - Implementing real-time/adaptive beamforming
    - matrix eigenvalue decomposition in FPGA's (Power iteration, Lanczos Alg.)
    - iterative update of ACM inverse (Woodbury's identity)
  - Tied-array processor for ASKAP (second-stage beamformer + GPU post-proc.)
  - Efficient oversampled synthesis filterbanks
  - RFI mitigation through time-gating (ADSB)
- High dynamic range RF-over-fiber
  - High-power laser drivers
  - Balanced/differential Mach-Zehnder modulators
  - Balanced InGaAs photodiodes

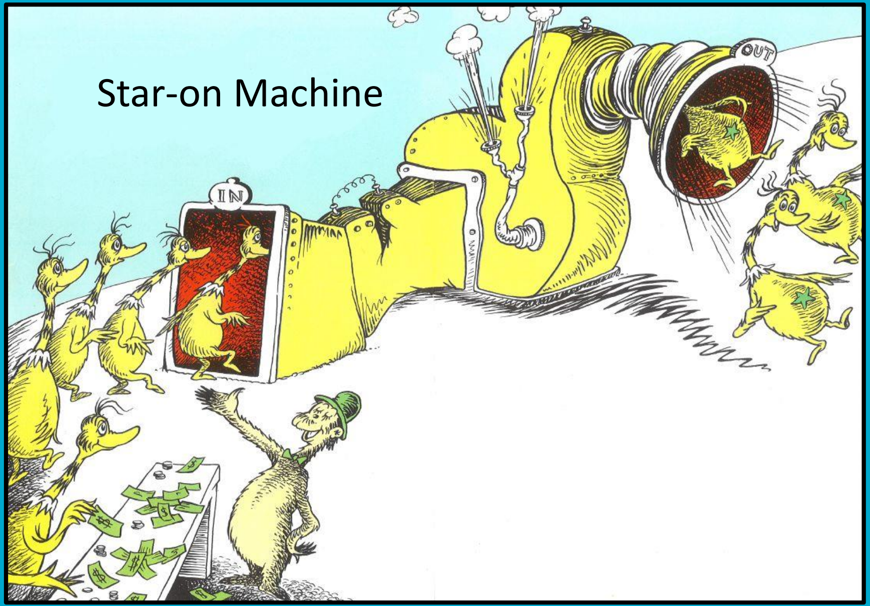
Serial interfaces (JESD204B)

Low frequency Optical-to-Digital Module (prototype)

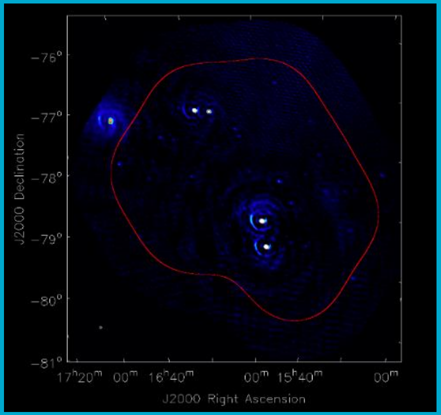


Power-over-fibre

- Full galvanic isolation for electronics
- Typical 45% optical-to-electrical conversion efficiency at 1W optical input levels
- 2W output power from single device
- Accepts 1W to 4.5W laser diode input power
- Constant output power with multi-mode fiber sizes from 62.5µm to 200µm
- Currently addressing safety aspects before we proceed further



Dr. Seuss - The Sneetches and Other Stories



Thank you

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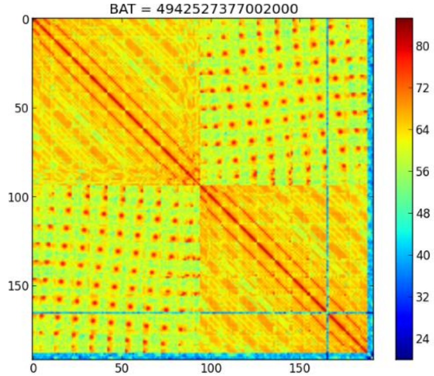
Beamforming Algorithm

- Maximum SNR with phase matching

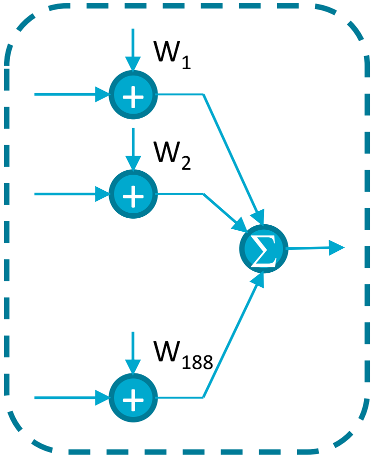
$$\left(\mathbf{R}_{s+n} - \mathbf{R}_n\right)v = \lambda w \Rightarrow \hat{w} = \mathbf{R}_n^{-1}\hat{v} \quad \text{(where } \hat{v} \leftrightarrow \lambda_{\max}\text{)}$$

weights modified for smooth phase: $\hat{w}' = e^{-j\phi}\hat{w} \quad \phi = \arg \hat{w}^H w_r$

Array covariance matrix



New beamformer weights



x 384 1MHz frequency channels

- other approaches…
  - sub-space projection (RFI mitigation, see next presentation!)
  - Shape-constrained beamforming